

JEE MAIN SEMICONDUCTOR ELECTRONICS — PYQS

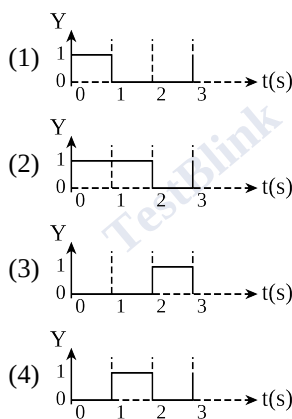
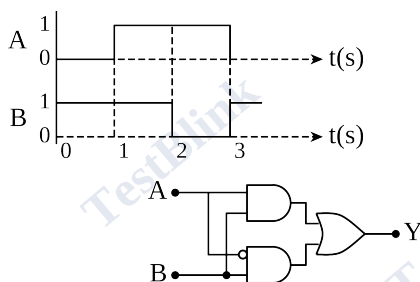
Max. Marks: 132

Questions: 33

Section A (MCQ) — 31 questions

Q.1 The output Y for the given inputs A and B to the circuit is :

[JEE Main 2026 (Online) 8th April Evening Shift]



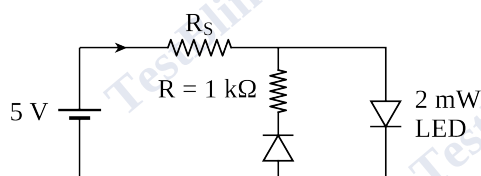
Scan or tap for the full solution



Q.2 The maximum rated power of the LED is 2 mW and it is used in the circuit with input voltage of 5 V as shown in the figure below. The current through resistance R_S is 0.5 mA.

The minimum value of the resistance of R_S , to ensure that the LED is not damaged is _____ k Ω .

[JEE Main 2026 (Online) 6th April Morning Shift]



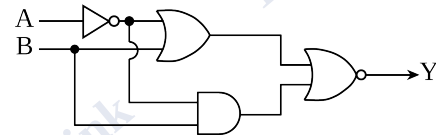
- (1) 6 (2) 2 (3) 4 (4) 5

Scan or tap for the full solution



Q.3 Refer to the logic circuit given below. For two inputs ($A = 1, B = 1$) and ($A = 0, B = 1$), output (Y) will be _____.

[JEE Main 2026 (Online) 6th April Evening Shift]



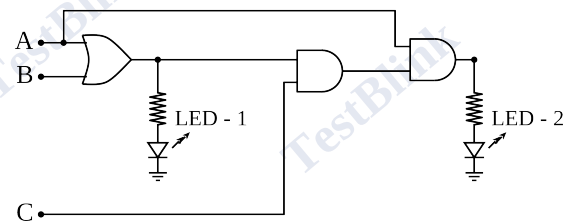
- (1) 1, 0 respectively (2) 0, 1 respectively
(3) 0, 0 respectively (4) 1, 1 respectively

Scan or tap for the full solution



Q.4 For the given logic circuit, which of the following inputs combination will make both LED-1 and LED-2 to glow?

[JEE Main 2026 (Online) 5th April Morning Shift]



- (1) $A = 0, B = 1, C = 1$ (2) $A = 1, B = 0, C = 0$
(3) $A = 1, B = 0, C = 1$ (4) $A = 1, B = 1, C = 0$

Scan or tap for the full solution



Q.5 In a semiconductor p-n diode, the doping concentrations on p-side and n-side are 10^{15} atoms/cm³ and 10^{18} atoms/cm³, respectively. Which one of the following statements is true ?

[JEE Main 2026 (Online) 5th April Evening Shift]

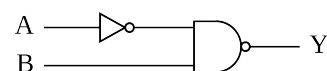
- (1) Widths of depletion region on either side of the interface are equal
(2) The depletion region width is more on p-side compared to that in n-side
(3) The depletion region width is more on n-side compared to that in p-side
(4) No depletion region forms because of unequal doping concentrations on p and n-sides

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Q.6 Two 4 bits binary numbers, $A = 1101$ and $B = 1010$ are given in the inputs of a logic circuit shown in figure below. The output (Y) will be :

[JEE Main 2026 (Online) 4th April Morning Shift]



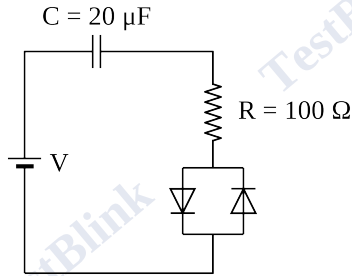
- (1) Y = 1101 (2) Y = 0010
 (3) Y = 0111 (4) Y = 1000

Scan or tap for the
full solution



- Q.7** Consider a circuit consisting of a capacitor ($20\ \mu\text{F}$), resistor ($100\ \Omega$) and two identical diodes as shown in figure. The resistance of diode under forward biasing condition is $10\ \Omega$. The time constant of the circuit is $\alpha \times 10^{-3}\ \text{s}$. The value of α is _____.

[JEE Main 2026 (Online) 4th April Morning Shift]



- (1) 2.2 (2) 2.0 (3) 2.1 (4) 2.4

Scan or tap for the
full solution



- Q.8** Given below are two statements: one is labelled as **Assertion (A)** and the other is labelled as **Reason (R)**.

Assertion (A): A diode under reverse-biased condition provides very small current which is nearly independent of voltage until a critical limit at which the current increases drastically.

Reason (R): Below the critical voltage limit, only majority charge carriers flow which increases drastically above critical voltage.

Choose the correct answer from the options given below : [JEE Main 2026 (Online) 4th April Evening Shift]

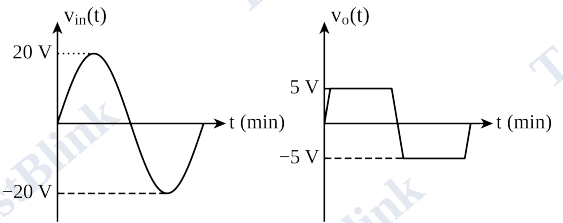
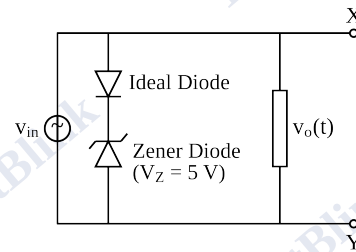
- (1) Both (A) and (R) are true and (R) is the correct explanation of (A)
 (2) Both (A) and (R) are true but (R) is NOT the correct explanation of (A)
 (3) (A) is true but (R) is false
 (4) (A) is false but (R) is true

Scan or tap for the
full solution



- Q.9** For the given circuit (shown in part (A)) the time dependent input voltage $v_{in}(t)$ and corresponding output $v_o(t)$ are shown in part (B) and part (C), respectively. Identify the components that are used in the circuit between points X and Y.

[JEE Main 2026 (Online) 2nd April Morning Shift]



Part (B): Input Voltage

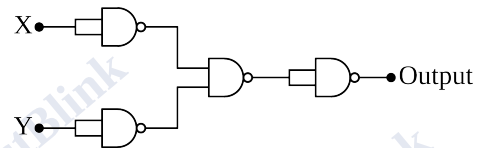
Part (C): Output Voltage

- (1) X ————> [Resistor] ————> [Diode] ————> Y
 (2) X ————> [Diode] ————> [Diode] ————> Y
 (3) X ————> [Resistor] ————> [Diode] ————> Y
 (4) X ————> [Diode] ————> [Diode] ————> Y

Scan or tap for the
full solution



- Q.10** If X and Y are the inputs, the given circuit works as _____. [JEE Main 2026 (Online) 2nd April Evening Shift]



- (1) OR gate (2) AND gate
 (3) NAND gate (4) NOR gate

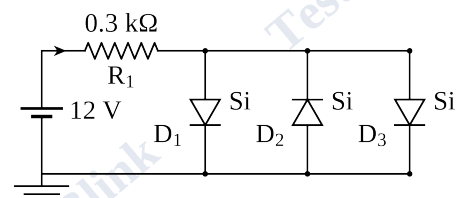
Scan or tap for the
full solution



- Q.11** Assuming in forward bias condition there is a voltage drop of $0.7\ \text{V}$ across a silicon diode, the current through diode D_1 in the circuit is _____ mA.

(Assume all diodes in the given circuit are identical)

[JEE Main 2026 (Online) 28th January Morning Shift]



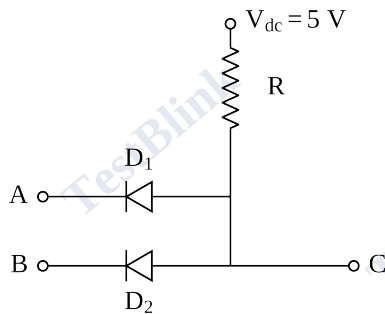
- (1) 17.6 (2) 18.8 (3) 20.15 (4) 11.7

Scan or tap for the
full solution



- Q.12** Two p-n junction diodes D_1 and D_2 are connected as shown in figure. A and B are input signals and C is the output. The given circuit will function as a _____.

[JEE Main 2026 (Online) 28th January Evening Shift]



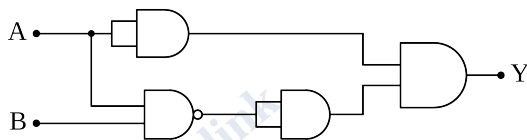
- (1) AND Gate (2) OR Gate
(3) NOR Gate (4) NAND Gate

Scan or tap for the full solution



- Q.13** Identify the correct truth table of the given logic circuit.

[JEE Main 2026 (Online) 24th January Evening Shift]



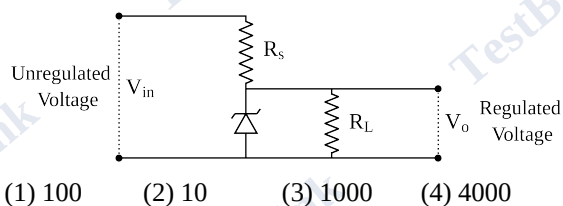
- | (1) | <table border="1"> <thead> <tr><th>A</th><th>B</th><th>Y</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table> | A | B | Y | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | (2) | <table border="1"> <thead> <tr><th>A</th><th>B</th><th>Y</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table> | A | B | Y | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | Y | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | B | Y | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| (3) | <table border="1"> <thead> <tr><th>A</th><th>B</th><th>Y</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table> | A | B | Y | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | (4) | <table border="1"> <thead> <tr><th>A</th><th>B</th><th>Y</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table> | A | B | Y | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| A | B | Y | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | B | Y | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Scan or tap for the full solution



- Q.14** The following diagram shows a Zener diode as a voltage regulator. The Zener diode is rated at $V_z = 5\text{ V}$ and the desired current in load is 5 mA . The unregulated voltage source can supply up to 25 V . Considering the Zener diode can withstand four times the load current, the value of resistor R_s (shown in circuit) should be _____ Ω .

[JEE Main 2026 (Online) 23rd January Morning Shift]



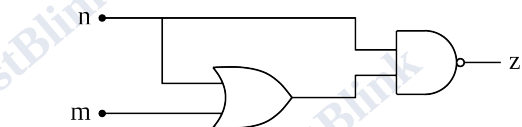
- (1) 100 (2) 10 (3) 1000 (4) 4000

Scan or tap for the full solution



- Q.15** For the given logic gate circuit, which of the following is the correct truth table?

[JEE Main 2026 (Online) 23rd January Evening Shift]



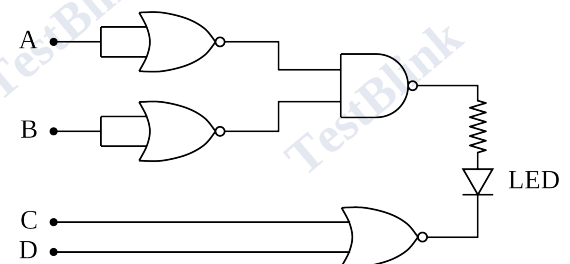
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|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| n | m | z | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| n | m | z | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| (3) | <table border="1"> <thead> <tr><th>n</th><th>m</th><th>z</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> </tbody> </table> | n | m | z | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | (4) | <table border="1"> <thead> <tr><th>n</th><th>m</th><th>z</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> </tbody> </table> | n | m | z | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| n | m | z | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| n | m | z | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Scan or tap for the full solution



- Q.16** Find the correct combination of A, B, C and D inputs which can cause the LED to glow.

[JEE Main 2026 (Online) 22nd January Morning Shift]



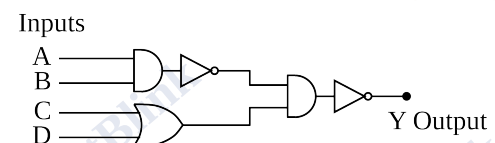
- (1) 1000 (2) 0011 (3) 0100 (4) 1101

Scan or tap for the full solution



- Q.17** The correct truth table for the given input data of the following logic gate is :

[JEE Main 2026 (Online) 22nd January Evening Shift]



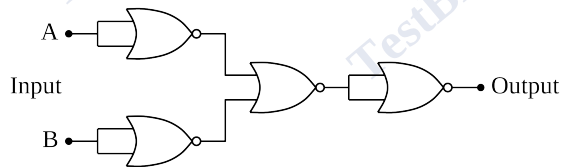
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|--------|---|--------|--------|-----|---|--------|--------|
| Inputs | Output | | | | | | |
| A | B | C | D | Y | | | | |
| 1 | 1 | 0 | 1 | 1 | | | | |
| 0 | 0 | 1 | 1 | 0 | | | | |
| 1 | 0 | 1 | 0 | 0 | | | | |
| 1 | 1 | 1 | 1 | 1 | | | | |
| Inputs | Output | | | | | | |
| A | B | C | D | Y | | | | |
| 1 | 1 | 0 | 1 | 0 | | | | |
| 0 | 0 | 1 | 1 | 1 | | | | |
| 1 | 0 | 1 | 0 | 1 | | | | |
| 1 | 1 | 1 | 1 | 1 | | | | |
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| Inputs | Output | | | | | | |
| A | B | C | D | Y | | | | |
| 1 | 1 | 0 | 1 | 1 | | | | |
| 0 | 0 | 1 | 1 | 0 | | | | |
| 1 | 0 | 1 | 0 | 1 | | | | |
| 1 | 1 | 1 | 1 | 0 | | | | |
| Inputs | Output | | | | | | |
| A | B | C | D | Y | | | | |
| 1 | 1 | 0 | 1 | 0 | | | | |
| 0 | 0 | 1 | 1 | 0 | | | | |
| 1 | 0 | 1 | 0 | 1 | | | | |
| 1 | 1 | 1 | 1 | 1 | | | | |

Scan or tap for the full solution



Q.18 The given circuit works as :

[JEE Main 2026 (Online) 21st January Morning Shift]



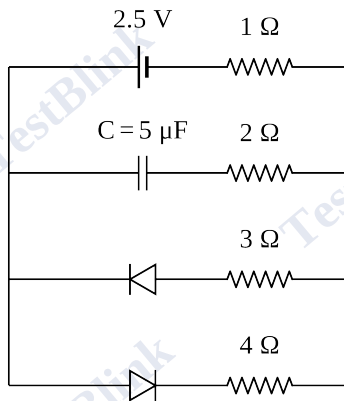
- (1) NOR gate (2) OR gate
(3) AND gate (4) NAND gate

Scan or tap for the full solution



Q.19 The charge stored by the capacitor C in the given circuit in the steady state is _____ μC .

[JEE Main 2026 (Online) 21st January Evening Shift]



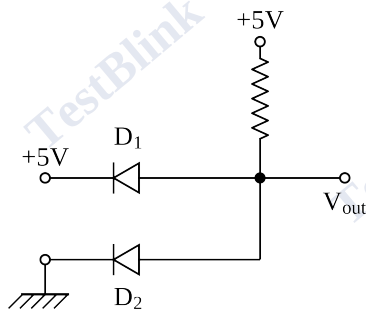
- (1) 7.5 (2) 5 (3) 10 (4) 12.5

Scan or tap for the full solution



Q.20 The output voltage in the following circuit is (Consider ideal diode case)

[JEE Main 2025 (Online) 8th April Evening Shift]



- (1) 0 V (2) +5 V (3) -5 V (4) 10 V

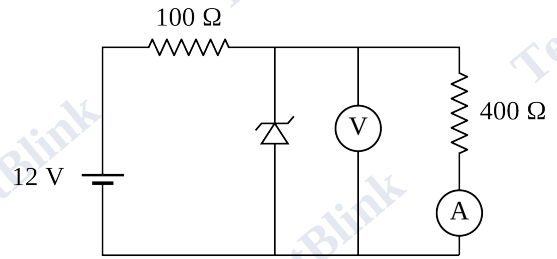
Scan or tap for the full solution



Q.21 In the following circuit, the reading of the ammeter will be

(Take Zener breakdown voltage = 4 V)

[JEE Main 2025 (Online) 7th April Morning Shift]

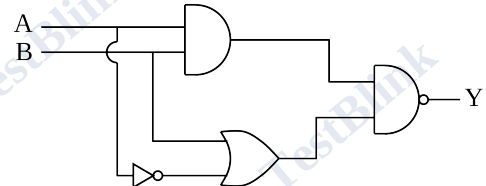


- (1) 60 mA (2) 80 mA (3) 10 mA (4) 24 mA

Scan or tap for the full solution



Q.22 Consider the following logic circuit.



The output is $Y = 0$ when :

[JEE Main 2025 (Online) 7th April Evening Shift]

- (1) $A = 1$ and $B = 0$ (2) $A = 0$ and $B = 0$
(3) $A = 1$ and $B = 1$ (4) $A = 0$ and $B = 1$

Scan or tap for the full solution



Q.23 The Boolean expression $Y = \overline{A}BC + \overline{A}\overline{C}$ can be realised with which of the following gate configurations.

- A. One 3-input AND gate, 3 NOT gates and one 2-input OR gate, one 2-input AND gate
B. One 3-input AND gate, 1 NOT gate, one 2-input NOR gate and one 2-input OR gate
C. 3-input OR gate, 3 NOT gates and one 2-input AND gate

Choose the correct answer from the options given below: [JEE Main 2025 (Online) 4th April Morning Shift]

- (1) B, C Only (2) A, B, C Only
(3) A, B Only (4) A, C Only

Scan or tap for the full solution



Q.24 Consider an n-type semiconductor in which n_e and n_h are number of electrons and holes, respectively.

- A. Holes are minority carriers
B. The dopant is a pentavalent atom
C. $n_e n_h \neq n_i^2$ (where n_i is number of electrons or holes in semiconductor when it is in intrinsic form)
D. $n_e n_h \geq n_i^2$
E. The holes are not generated due to the donors

Choose the correct answer from the options given below :

[JEE Main 2025 (Online) 4th April Evening Shift]

- (1) (A), (B), (E) only (2) (A), (C), (E) only
(3) (A), (B), (C) only (4) (A), (C), (D) only

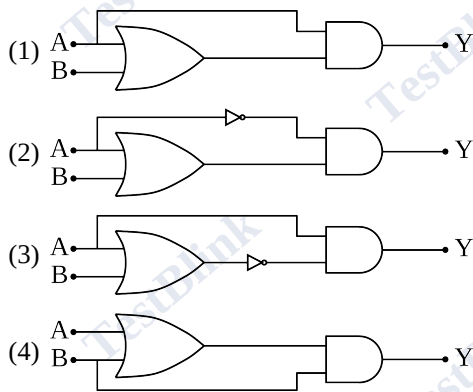
Scan or tap for the full solution



Q.25 Choose the correct logic circuit for the given truth table having inputs A and B.

[JEE Main 2025 (Online) 3rd April Morning Shift]

Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

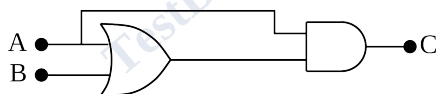


Scan or tap for the full solution



Q.26 The truth table corresponding to the circuit given below is:

[JEE Main 2025 (Online) 3rd April Evening Shift]



(1)	A	B	C
	0	0	0
	0	1	0
	1	0	1
	1	1	1

(2)	A	B	C
	0	0	1
	1	0	0
	0	1	0
	1	1	0

(3)	A	B	C
	0	0	1
	0	1	0
	1	0	0
	1	1	0

(4)	A	B	C
	0	0	0
	1	0	0
	0	1	0
	1	1	1

Scan or tap for the full solution



Q.27 A zener diode with 5 V zener voltage is used to regulate an unregulated dc voltage input of 25 V. For a 400 Ω resistor connected in series, the zener current is found to be 4 times load current. The load current (I_L) and load resistance (R_L) are :

[JEE Main 2025 (Online) 2nd April Morning Shift]

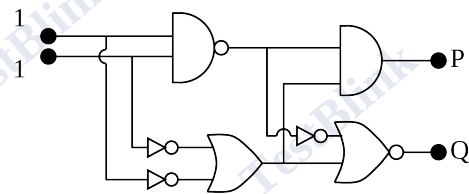
- (1) $I_L = 0.02$ mA; $R_L = 250$ Ω
- (2) $I_L = 10$ A; $R_L = 0.5$ Ω
- (3) $I_L = 10$ mA; $R_L = 500$ Ω
- (4) $I_L = 20$ mA; $R_L = 250$ Ω

Scan or tap for the full solution



Q.28 In the digital circuit shown in the figure, for the given inputs the P and Q values are :

[JEE Main 2025 (Online) 2nd April Evening Shift]

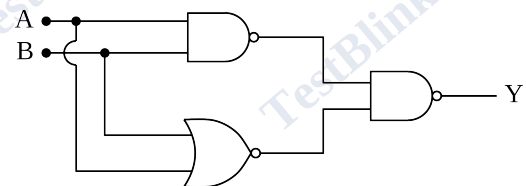


- (1) P = 0, Q = 1
- (2) P = 1, Q = 0
- (3) P = 0, Q = 0
- (4) P = 1, Q = 1

Scan or tap for the full solution



Q.29



For the circuit shown above, equivalent GATE is :

[JEE Main 2025 (Online) 29th January Morning Shift]

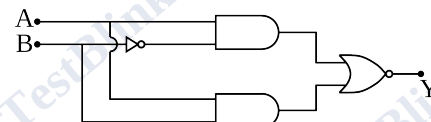
- (1) NOT gate
- (2) NAND gate
- (3) AND gate
- (4) OR gate

Scan or tap for the full solution



Q.30 Which of the following circuits has the same output as that of the given circuit?

[JEE Main 2025 (Online) 28th January Morning Shift]

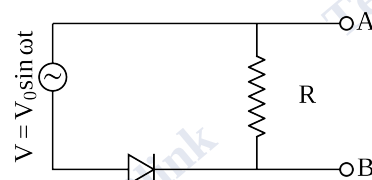


- (1)
- (2)
- (3)
- (4)

Scan or tap for the full solution

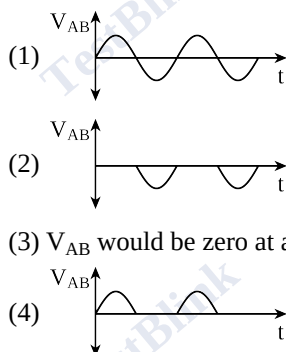


Q.31



In the circuit shown here, assuming threshold voltage of diode is negligibly small, then voltage V_{AB} is correctly represented by:

[JEE Main 2025 (Online) 28th January Evening Shift]



Scan or tap for the full solution



Section B (Numerical) — 2 questions

Q.32 A diode has Zener voltage of 10 V and maximum power dissipation of 0.5 W, then the minimum resistance to be used in series with this diode for safety when it is connected to a 25 V power supply is _____ Ω .

[JEE Main 2026 (Online) 4th April Evening Shift]

Scan or tap for the full solution



Q.33 A voltage regulating circuit consisting of Zener diode, having breakdown voltage of 10 V and maximum power dissipation of 0.4 W, is operated at 15 V. The approximate value of protective resistance in this circuit is _____ Ω .

[JEE Main 2026 (Online) 24th January Morning Shift]

Scan or tap for the full solution



ANSWER KEY

Section A (MCQ) — 31 questions

Ques.	1	2	3	4	5	6	7	8	9	10	11
Ans.	2	2	3	3	2	1	1	3	2	4	2
Ques.	12	13	14	15	16	17	18	19	20	21	22
Ans.	1	1	3	1	4	1	4	3	1	3	3
Ques.	23	24	25	26	27	28	29	30	31		
Ans.	3	1	1	1	3	3	4	1	2		

Section B (Numerical) — 2 questions

Ques.	32	33					
Ans.	300	125					